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polysilicon layer and a second undoped polysilicon layer, and a first metal pattern formed deposited over the upper electrode.

REMARKS

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1d of the present application in view of Chen, *et al.* (U.S. Patent No. 6,033,950). Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1d of the present application in view of Chen, *et al.* and further in view of Hanagasaki (U.S. Patent No. 5,767,541). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the applicants' invention, a capacitor structure includes an upper electrode which includes a three-layer deposition structure. The three-layer structure includes a doped polysilicon layer between first and second undoped polysilicon layers. The upper undoped polysilicon layer is formed immediately adjacent to a metal layer used in forming the upper electrode of the capacitor. Undoped polysilicon is used as the upper layer interface with the metal layer to provide a thicker adhesion layer between the metal layer and the polysilicon to prevent lifting of the metal layer.

The claims are amended to explicitly recite additional structural features of the applicants' invention. Specifically, the claims are amended to recite the metal pattern formed over the first electrode.

In contrast to the applicants' claimed invention, in the structure illustrated in Figure 1d of the application and described in the applicants' Background of the Invention section, the polysilicon pattern in the capacitor electrode is a two-layer pattern which includes a lower undoped polysilicon layer and an upper doped polysilicon layer. A metal pattern is formed over the upper doped polysilicon. During subsequent processes such as an annealing process, a silicide layer is formed between the polysilicon layer and the metal layer, resulting in improved

adhesion between the metal layer and the polysilicon. However, adhesion between the silicon and the metal layer is determined by the degree to which the metal and silicon react during annealing. The thickness of the resulting silicide layer is inversely proportional to the doping layer of the polysilicon in contact with the metal layer. Thus, the high impurity concentration in the polysilicon layer results in a relatively thinner silicide layer, which, in turn, results in reduced adhesion between the metal and the polysilicon.

Hence, the applicants' improvement over the prior art device involves reducing the impurities in the layer contacting the metal. This results in a thicker layer being formed between the two during the annealing process, which results in better adhesion.

In Chen, *et al.*, as the Examiner notes, an undoped polysilicon layer 34 is formed on a doped polysilicon layer 32 to form an electrode of a capacitor. The upper undoped polysilicon layer 34 is used to reduce out-diffusion of impurities from the lower doped polysilicon during thermal cycles, thus preventing auto doping. In auto doping, the dopant diffuses out of the polysilicon and reaches the surface of the device and diffuses into the substrate during subsequent thermal processes. In other devices formed on the same wafer, the out-diffused dopant laterally and vertically increase the other dopant concentrations near or under edges of channel regions of adjacent devices. The undoped polysilicon layer 34 is placed on top of the doped polysilicon layer 32 to prevent this out-diffusion of dopant.

There is no motivation found in either prior art reference device for combining the applicants' admitted prior art device with Chen, *et al.* Chen, *et al.* does not suggest any motivation for adding an undoped polysilicon layer to the prior art device of Figure 1d.

To establish a prima facie case of obviousness, the prior art reference or references when combined must not only teach or suggest all the recitations of the claim, there must also be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combined reference teachings. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the

combination. To support combining references, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement for clear and particular evidence is not met by broad and conclusory statements about the teachings of the reference. To support combining or modifying references, there must be particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.

The applicants respectfully submit that the present rejections set forth in the Office Action fail to meet the requirements for combining the references in the manner relied on to show obviousness. While Chen *et al.* do disclose a capacitor structure comprising a deposition structure including two layers including an upper electrode with an undoped polysilicon layer 34 formed on a doped polysilicon layer 32 to prevent out-diffusion from the lower doped polysilicon layer 32, they do not disclose or suggest the upper electrode comprising a deposition structure including three layers, including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer, and a first metal pattern formed deposited over the upper electrode, as presented in amended claim 1.

Both the applicants' admitted prior art device and the device of Chen *et al.* include two-layer deposition structures. The Chen *et al.* structure is a two-layer structure with undoped polysilicon over doped polysilicon. The applicants' admitted prior art device is a two-layer structure with undoped polysilicon over doped polysilicon and a metal pattern over the two-layer structure. There is no suggestion in either reference of three-layer structures or any possible benefit to a three-layer structure. Also, Chen, *et al.* does not at all contemplate adhesion of a metal layer, since the undoped polysilicon layer of Chen, *et al.* is adjacent to a thick insulating layer 40, not a metal conductive layer. The applicants respectfully submit that there is no motivation suggested by either reference of combining two-layer structure under a metal pattern with a two-layer structure under an insulator to obtain a three-layer structure under a metal pattern, as claimed by the applicants.

Since there would be no motivation for one of skill in the art to combine the structure of Figure 1d of the application with the teachings of Chen, *et al.* to obtain a three-layer deposition

structure as claimed by the applicants, it is believed that the rejection of the claims under 35 U.S.C. § 103(a) based on the combination of Figure 1d and Chen, *et al.* is improper. Accordingly, reconsideration of the rejections of the claims based on Figure 1d of the application, Chen, *et al.* and Hanagasaki is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 10/24/02

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774

Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Version with Markings to Show Changes Made

In the Claims

Claim 4 has been canceled.

Claim 1 has been amended as follows:

1. (Twice Amended) A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including three layers including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer, and a first metal pattern formed deposited over the upper electrode.

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